

CLAIMS

What is claimed is:

1. A circuit for generating a spread spectrum clock comprising:  
5           an output node;  
              a voltage controller oscillator (VCO) that includes an input  
              coupled to a voltage control node ( $V_{ctrl}$ ) for receiving a  
              voltage signal and an output for generating a clock signal  
              that has a frequency ( $F_{out}$ ) dependent on the received  
10           voltage signal; and

15           a VCO input voltage modulation mechanism, coupled to the  
              VCO input voltage node, for modulating the voltage at  
              the VCO input voltage node to generate a spread  
              spectrum clock.

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2. The circuit of claim 1 wherein the VCO input voltage modulation  
mechanism further includes

20           a voltage shift-up mechanism for pulling up the voltage at the  
              VCO input voltage node by injecting a level shifting current into the  
              VCO input voltage node.

3. The circuit of claim 2 wherein the VCO input voltage modulation  
mechanism further includes

25           a modulation control circuit for generating shift-up control enable  
              signal and at least one shift-up control signal for use in controlling the  
              voltage shift-up mechanism;

wherein the voltage shift-up mechanism includes a first input for receiving the shift-up control enable signal and a second input for receiving shift-up control signal.

5 4. The circuit of claim 1 wherein the VCO input voltage modulation mechanism further includes

a voltage shift-down mechanism for pulling down the voltage at the VCO input voltage node by drawing a level shifting current from the VCO input voltage node.

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5. The circuit of claim 4 wherein the VCO input voltage modulation mechanism further includes

a modulation control circuit for generating shift-down control enable signal and at least one shift-down control signal for use in controlling the voltage shift-down mechanism;

15 wherein the voltage shift-down mechanism includes a first input for receiving the shift-down control enable signal and a second input for receiving shift-down control signal.

20 6. The circuit of claim 2 wherein the voltage shift-up mechanism includes

a first transistor having a drain electrode coupled to a first predetermined voltage, a source electrode, and a gate electrode for receiving a first shift-up control signal;

25 a second transistor having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to the VCO

input voltage node, and a gate electrode for receiving a shift-up control enable signal.

7. The circuit of claim 6 wherein the voltage shift-up mechanism

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a plurality of transistors coupled in parallel to the first transistor;

wherein each transistor includes a drain electrode that is coupled to the first predetermined voltage, a source electrode that is coupled to the drain electrode of the second transistor, and a gate electrode for 10 receiving a corresponding shift-up control signal.

8. The circuit of claim 2 wherein the voltage shift-down mechanism

includes

a first transistor having a drain electrode coupled to the VCO 15 input voltage node, a source electrode, and a gate electrode for receiving a shift-down control enable signal;

a second transistor having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to a second predetermined voltage, and a gate electrode for receiving a shift-down 20 control signal.

9. The circuit of claim 8 wherein the voltage shift-down mechanism

includes

a plurality of transistors coupled in parallel to the second 25 transistor;

wherein each transistor includes a drain electrode that is coupled to the source of the first transistor, a source electrode that is coupled to the second predetermined voltage, and a gate electrode for receiving a corresponding shift-down control signal.

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10. The circuit of claim 1 integrated in one of personal computers (PCs), computing devices, computer peripherals, office equipment, printers, network equipment, and other electronic applications where EMI reduction is needed.

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11. The circuit of claim 1 wherein the modulation control circuit includes a plurality of programmable delay cells (PDCs) for generating the shift-up control signals and the shift-down control signals; wherein the time delay ( $\Delta(t)$ ) of the delay cells is based on the modulation frequency ( $F_{mod}$ ) and the number of modulation bits.

12. The circuit of claim 11 wherein the circuit includes a phase locked loop (PLL).

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13. The circuit of claim 12 wherein the time delay of the delay cells are also determined by stability considerations for the PLL and the VCO characterization.

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14. The circuit of claim 12 wherein the delay cells are implemented as one of software and hardware.

15. A method for reducing electromagnetic interference (EMI) in a clock generation circuit that includes a VCO input voltage modulation mechanism, coupled to a VCO input voltage node, for modulating the voltage at the VCO input voltage node comprising the steps of:

- 5        a) configuring the VCO input voltage modulation mechanism;
- b) adjusting the VCO input voltage in a first direction to cause the frequency of the output of the PLL circuit to change in a first direction; and
- c) adjusting the VCO input voltage in a second direction to cause  
10          the frequency of the output of the PLL circuit to change in a second direction.

16. The method of claim 15 wherein the clock generation circuit includes a voltage controlled oscillator (VCO) that includes an output,  
15          wherein the method further comprises the step of:

repeating steps (b) and (c) to modulate the VCO output to reduce electromagnetic interference (EMI) of the clock signal generation circuit.

- 20        17. The method of claim 15 wherein the step of adjusting the VCO input voltage in a first direction to cause the frequency of the output of the PLL circuit to change in a first direction includes  
            injecting a voltage level shifting current into the VCO input voltage node.

18. The method of claim 15 wherein the step of adjusting the VCO input voltage in a second direction to cause the frequency of the output of the PLL circuit to change in a second direction includes

5 drawing a voltage level shifting current from the VCO input voltage node.

19. The method of claim 15 further comprising the step of:  
employing a P-counter that has a single value.

10 20. The circuit of claim 1 further comprising:  
a P-counter that includes an input coupled to the VCO, a register  
for storing a single P value and an output;  
a Q-counter that includes an input for receiving a reference  
frequency ( $F_{in}$ ) and an output;  
15 a phase detector that includes a first input coupled to the output  
of the Q counter ( $F_{ref}$ ) and a second input coupled to the  
output of the P counter ( $F_{fb}$ ) and an output for  
generating a control signal;  
a charge pump coupled to the phase detector for receiving the  
20 control signal and selectively charging and discharging  
the voltage control node based on the control signal; and  
a loop filter.